M.Tech in Electronics & Communication Engineering w.e.f. 2011-2012

Deptt. of Electronics & Communication Engineering

Guru Jambheshwar University of Science & Technology, Hisar
### First Semester

**List of Compulsory/Core Courses**

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Course Title</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td>ECL-712</td>
<td>IC Fabrication Technology</td>
<td>4</td>
</tr>
<tr>
<td>ECL-713</td>
<td>Digital VLSI Design</td>
<td>4</td>
</tr>
<tr>
<td>ECL-714</td>
<td>Hardware Description Languages</td>
<td>4</td>
</tr>
<tr>
<td>ECL-715</td>
<td>Embedded System Design</td>
<td>4</td>
</tr>
<tr>
<td>ECL-719</td>
<td>Signal Processing</td>
<td>4</td>
</tr>
<tr>
<td>ECP-716</td>
<td>Digital VLSI Design Lab</td>
<td>2</td>
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<tr>
<td>ECP-717</td>
<td>HDL Lab</td>
<td>2</td>
</tr>
<tr>
<td>ECP-718</td>
<td>Embedded System Design Lab</td>
<td>2</td>
</tr>
</tbody>
</table>

**Total Credits** 26

### Second Semester

**List of Compulsory/Core Courses**

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Course Title</th>
<th>Credits</th>
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</thead>
<tbody>
<tr>
<td>ECL-721</td>
<td>Mobile Communication</td>
<td>4</td>
</tr>
<tr>
<td>ECL-722</td>
<td>Advanced Optical Communication Systems</td>
<td>4</td>
</tr>
<tr>
<td>ECL-723</td>
<td>Analog IC Design</td>
<td>4</td>
</tr>
<tr>
<td>ECL-724</td>
<td>Adaptive Signal Processing</td>
<td>4</td>
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<tr>
<td></td>
<td>Elective-I</td>
<td>4</td>
</tr>
<tr>
<td>ECP-726</td>
<td>Adaptive Signal Processing Lab</td>
<td>2</td>
</tr>
<tr>
<td>ECP-727</td>
<td>Advanced Communication Lab</td>
<td>2</td>
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</table>

**Total Credits** 24

**List of Electives -I**: The student can opt any one elective from the following list.

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Course Title</th>
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</thead>
<tbody>
<tr>
<td>ECL-725 (i)</td>
<td>Algorithms for VLSI Design Automation</td>
</tr>
<tr>
<td>ECL-725 (ii)</td>
<td>Advanced Computer Architecture</td>
</tr>
<tr>
<td>ECL-725 (iii)</td>
<td>MEMS and IC Integration</td>
</tr>
</tbody>
</table>

### Third Semester

**List of Compulsory/Core Courses**

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Course Title</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td>ECP-732</td>
<td>Advance VLSI Design Lab</td>
<td>2</td>
</tr>
<tr>
<td>ECP-733</td>
<td>Communication System Design Lab</td>
<td>2</td>
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<tr>
<td>ECD-730</td>
<td>Thesis – Part I with Seminar</td>
<td>3</td>
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</tbody>
</table>

**Total Credits** 11
**List of Electives- II:** The student can opt one elective from the following list.

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Course Title</th>
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<tbody>
<tr>
<td>ECL-731 (i)</td>
<td>Mixed-Signal Design</td>
</tr>
<tr>
<td>ECL-731 (ii)</td>
<td>RF Micro-electronics</td>
</tr>
<tr>
<td>ECL-731 (iii)</td>
<td>VLSI Testing And Testability</td>
</tr>
<tr>
<td>ECL-731 (iv)</td>
<td>Memory System Design</td>
</tr>
<tr>
<td>ECL-731 (v)</td>
<td>Low Power VLSI Design</td>
</tr>
<tr>
<td>ECL-731 (vi)</td>
<td>Embedded System for Wireless &amp; Mobile Communication</td>
</tr>
<tr>
<td>ECL-731 (vii)</td>
<td>Hardware &amp; Software Co-Design</td>
</tr>
<tr>
<td>ECL-731 (viii)</td>
<td>Advanced Digital Communication</td>
</tr>
<tr>
<td>ECL-731 (ix)</td>
<td>Satellite Communication</td>
</tr>
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**Fourth Semester**

<table>
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<tr>
<th>Course Code</th>
<th>Course Title</th>
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<tbody>
<tr>
<td>ECD-740</td>
<td>Thesis – Part II</td>
<td>09</td>
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</table>

**Total Credits** 09

- 04 contact Hrs per week are required for each theory subject including electives.
- 04 contact Hrs per week are required for each Lab.
- 02 Hrs per student per week teaching load will be assigned for thesis work.
  for Part I and Part II.

<table>
<thead>
<tr>
<th>Semester</th>
<th>Total Credits</th>
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<tbody>
<tr>
<td>I.</td>
<td>26</td>
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<tr>
<td>II.</td>
<td>24</td>
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<tr>
<td>III.</td>
<td>11</td>
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<tr>
<td>IV.</td>
<td>09</td>
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<tr>
<td>Grand Total</td>
<td>70 Credits</td>
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</table>
DETAILED SYLLABUS

M.Tech. (ECE)
FIRST SEMESTER

ECL-712  |  IC Fabrication Technology

Environment for VLSI Technology: Clean room and safety requirements. Wafer cleaning processes and wet chemical etching techniques.

Impurity incorporation: Solid State diffusion modelling and technology; Ion Implantation modelling, technology and damage annealing; characterisation of Impurity profiles.

Oxidation: Kinetics of Silicon dioxide growth both for thick, thin and ultrathin films. Oxidation technologies in VLSI and ULSI; Characterisation of oxide films; High k and low k dielectrics for ULSI.

Lithography: Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI; Mask generation.

Chemical Vapour Deposition techniques: CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal films; Epitaxial growth of silicon; modelling and technology.

Metal film deposition: Evaporation and sputtering techniques. Failure mechanisms in metal interconnects; Multi-level metallisation schemes.

Plasma and Rapid Thermal Processing: PECVD, Plasma etching and RIE techniques; RTP techniques for annealing, growth and deposition of various films for use in ULSI. Process integration for NMOS, CMOS and Bipolar circuits; Advanced MOS technology.

Texts/References:

Note: Examiner will set eight questions fairly distributed & covering the whole syllabus. Students will be required to attempt any five questions in the duration of 03 hours.
ECL-713 | Digital VLSI Design

1. Introduction to MOSFETs: MOS Transistor Theory - Introduction MOS Device, Fabrication and Modeling, Body Effect, Noise Margin; Latch-up

2. MOS Inverter: MOS Transistors, MOS Transistor Switches, CMOS Logic, Circuit and System Representations, Design Equations, Static Load MOS Inverters, Transistor Sizing, Static and Switching Characteristics; MOS Capacitor; Resistivity of Various Layers.


5. Sequential MOS Logic Circuits: SR Latch, clocked Latch and flip flop circuits, CMOS D latch and edge triggered flip flop.

6. Dynamic Logic Circuits; Basic principle, nonideal effects, domino CMOS Logic, high performance dynamic CMOS Circuits, Clocking Issues, Two phase clocking.

7. CMOS Subsystem Design: Semiconductor memories, memory chip organization, RAM Cells, dynamic memory cell.

TEXT BOOKS:


REFERENCE BOOKS:

Note: Examiner will set eight questions fairly distributed & covering the whole syllabus. Students will be required to attempt any five questions in the duration of 03 hours.

ECL-714 | Hardware Description Languages

2. **VHDL Background**: VHDL History, Existing Languages, VHDL Requirements, The VHDL Language.
3. **Design Methodology Based On VHDL**: Elements of VHDL, Top down Design, Top down Design with VHDL, Subprograms, Controller Description, VHDL Operators, Conventions and Syntax.
4. **Basic Concepts In VHDL**: Characterizing Hardware Languages, Objects and Classes, Signal Assignments, Concurrent and Sequential Assignments.
6. **Utilities For High-Level Descriptions**: Type Declarations and Usage, VHDL Operators, Subprogram Parameter Types and Overloading, Other Types and Type Related Issues, Predefined Attributes, User Defined Attributes.
7. **Dataflow Descriptions In VHDL**: Multiplexing and Data Selection, State Machine Description, Three State Bussing.
9. **Verilog**: Overview of Digital design with Verilog HDL, Hierarchical modeling concepts, basic concepts, modules & ports.

**TEXT BOOKS:**


**REFERENCE BOOKS:**

ECL-715  Embedded System Design

Introduction to Embedded systems design:
Introduction to Embedded system, Embedded System Project Management, ESD and Co-design issues in System development Process, Design cycle in the development phase for an embedded system, Use of target system or its emulator and In-circuit emulator, Use of software tools for development of an ES.

8051 Microcontroller: Microprocessor V/s Microcontroller, 8051 Microcontroller: General architecture; Memory organization; I/O pins, ports & circuits; Counters and Timers; Serial data input/output; Interrupts.


8051 Interfacing and Applications: Interfacing External Memory, Keyboard and Display Devices: LED, 7-segment LED display, LCD.

Advanced Microcontrollers: Only brief general architecture of AVR, PIC and ARM microcontrollers; JTAG: Concept and Boundary Scan Architecture.

Text Books:

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ECL-719  Signal Processing


3 Time Delay Estimation: Need for the Time Delay Estimation, System Model, Source Localization strategies, Ideal Model-Free field environment, TDE METHODS: Cross-correlation Function (CCF) method, Least mean square (LMS) adaptive filter method, Average square difference function (ASDF) method, Relation between the SNR level and the time delay estimation.


5. System modeling and identification: System identification based on FIR (MA), All Pole (AR), Pole Zero (ARMA) system models, Least square linear prediction filter, FIR least squares inverse filter, predictive deconvolution, Matrix formulation for least squares estimation: Cholesky decomposition, LDU decomposition, QRD decomposition, Graham V Schmidt orthogonalization.

BOOKS:
3. Harry L. Van Trees, “

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<table>
<thead>
<tr>
<th>ECP-716</th>
<th>Digital VLSI Design Lab</th>
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<tr>
<td></td>
<td>Experiments related to theory ECL-713.</td>
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<tr>
<th>ECP-717</th>
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<td></td>
<td>Experiments related to theory ECL-715.</td>
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</table>
SECOND SEMESTER

ECL-721   MOBILE COMMUNICATION

Introduction to Wireless Communication Systems: Various Generations of wireless mobile communication, The Cellular Concept, Frequency reuse, channel assignment strategies, hand-off strategies, interference and system capacity, improving capacity of cellular system through cell splitting, sectoring, etc.

Mobile Radio Propagation: Introduction to radio wave propagation, three basic propagation mechanisms, Outdoor & indoor propagation models, small scale multipath propagation, parameters of mobile multipath channel, small scale & large scale fading, their types.

Principles of GSM: GSM frequency bands, GSM architecture, GSM Interfaces, GSM logical channels and frame structure, GSM bursts, GPRS.


Implementation Issues: OFDM, Multi-Carrier Modulation and Demodulation, Channel Coding and Decoding (Convolutional codes, Turbo codes), Multi-user Detection: Decorrelating detector, MMSE detector. Successive Interference Canceller, Parallel Interference Canceller.

Text Books:
2. Wireless and Digital Communications; Dr. Kamilo Feher (PHI)
4. Wireless Communication; Principles and Practice; T.S.Rappaport

Note: Examiner will set eight questions fairly distributed & covering the whole syllabus. Students will be required to attempt any five questions in the duration of 03 hours.

ECL-722   Advanced Optical Communication Systems

**Fiber Optic System Design Considerations and Components Components:** Indoor Cables, Outdoor Cables, Cabling Example, Power Budget, Bandwidth and Rise Time Budgets, Electrical and Optical Bandwidth, Connectors, Fiber Optic Couplers.

Dispersion and Nonlinearities Dispersion in single mode and multimode fibers, dispersion shifted and dispersion flattened fibers, attenuation and dispersion limits in fibers, Kerr nonlinearity, self phase modulation, Cross Phase Modulation, FWM.

**Optical Sources:** optical source properties, operating wavelength of optical sources, semiconductor light-emitting diodes and laser diodes, semiconductor material and device operating principles, light-emitting diodes, surface-emitting LEDS, edge-emitting LEDS, super luminescent diodes, laser diodes, comparison of LED and ILD. Fiber optic transmitters, basic optical transmitters, direct versus external modulation, fiber optic transmitter applications.

**Optical Detectors:** Basic Information on light detectors, Role of an optical detector, Detector characteristics: Responsivity, Noise Equivalent Power, Detectivity, Quantum efficiency, The PN junction photo diode - PIN photodetectors - Avalanche photo diode construction characteristics and properties, APD Specifications, Applications of APD, Optical Receivers

**Advanced Multiplexing Strategies:** Optical TDM, subscriber multiplexing (SCM), WDM and Hybrid multiplexing methods.

**Optical Networking:** Data communication networks, network topologies, MAC protocols, Network Architecture- SONET/TDH, optical transport network, optical access network, optical premise network

**Books:**
3. John Gowar, Optical communication systems, PHI.

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**ECL-723 | Analog IC Design**

**Small Signal & large signal Models** of MOS & BJT transistor.

**MOS & BJT Transistor Amplifiers:** Single transistor Amplifiers stages: Common Emitter, Common base, Common Collector, Common Drain, Common Gate & Common Source Amplifiers

**Multiple Transistor Amplifier stages:** CC-CE, CC-CC, & Darlington configuration, Cascode configuration, Active Cascode. Differential Amplifiers: Differential pair & DC transfer characteristics.

**Current Mirrors, Active Loads & References**

Current Mirrors: Simple current mirror, Cascade current mirrors Widlar current mirror, Wilson Current mirror, etc. Active loads, Voltage & current references. Analysis of Differential Amplifier with active load, supply and temperature independent biasing techniques.
**Operational Amplifier:** Applications of operational Amplifier, theory and Design; Definition of Performance Characteristics; Design of two stage MOS Operational Amplifier, two stage MOS operational Amplifier with cascodes, MOS telescopic-cascode operational amplifiers, MOS Folded-cascode operational amplifiers, Bipolar operational amplifiers. Frequency response & compensation.

**Nonlinear Analog Circuits:** Voltage controlled oscillator, Comparators, Analog Buffers, Source Follower and Other Structures. Phase Locked Techniques; Phase Locked Loops (PLL), closed loop analysis of PLL. Digital-to-Analog (D/A) and Analog-to-Digital (A/D) Converters.

**OTA & Switched Capacitor filters**
OTA Amplifiers, Switched Capacitor Circuits and Switched Capacitor Filters.

**Text:**

**References:**

**Note:** Examiner will set eight questions fairly distributed & covering the whole syllabus. Students will be required to attempt any five questions in the duration of 03 hours.

**ECL-724 Adaptive Signal Processing**


**BOOKS:**

**Note:** Examiner will set eight questions fairly distributed & covering the whole syllabus. Students will be required to attempt any five questions in the duration of 03 hours.

**ELECTIVE-I**

The student can opt any one elective from the following list.

| ECL-725 (i) | Algorithm for VLSI Design Automation |

**Logic synthesis & verification:**
Introduction to combinational logic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis.

**VLSI automation Algorithms:**
**Partitioning:** problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms.

**Placement, floor planning & pin assignment:** problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment.

**Global Routing:** Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches.

**Detailed routing:** problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms.

**Over the cell routing & via minimization:** two layers over the cell routers, constrained & unconstrained via minimization

**Compaction:** problem formulation, one-dimensional compaction, two dimension based compaction, hierarchical compaction
Text Books:

References

Note: Examiner will set eight questions fairly distributed & covering the whole syllabus. Students will be required to attempt any five questions in the duration of 03 hours.

<table>
<thead>
<tr>
<th>ECL-725(ii)</th>
<th>Advanced Computer Architectures</th>
</tr>
</thead>
</table>

Parallel computer models: The state of computing, Classification of parallel computers, Multiprocessors and multicomputers, Multivector and SIMD computers.

Program and network properties: Conditions of parallelism, Data and resource Dependences, Hardware and software parallelism, Program partitioning and scheduling, Grain Size and latency, Program flow mechanisms, Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms

System Interconnect Architectures: Network properties and routing, Static interconnection Networks, Dynamic interconnection Networks, Multiprocessor system Interconnects, Hierarchical bus systems, Crossbar switch and multiport memory, Multistage and combining network.


Memory Hierarchy Design: Cache basics & cache performance, reducing miss rate and miss penalty, multilevel cache hierarchies, main memory organizations, design of memory hierarchies.

Multiprocessor architectures: Symmetric shared memory architectures, distributed shared memory architectures, models of memory consistency, cache coherence protocols (MSI, MESI, MOESI), scalable cache coherence, overview of directory based approaches, design challenges of directory protocols, memory based directory protocols, cache based directory protocols, protocol design tradeoffs, synchronization,

Scalable point –point interfaces: Alpha364 and HT protocols, high performance signaling layer.

Enterprise Memory subsystem Architecture: Enterprise RAS Feature set: Machine check, hot add/remove, domain partitioning, memory mirroring/migration, patrol scrubbing, fault tolerant system.

Text:
1. Kai Hwang, “Advanced computer architecture”; TMH.

References:
1. J.P.Hayes, “computer Architecture and organization”; MGH.
3. V.Rajaranam & C.S.R.Murthy, “Parallel computer”; PHI.

Note: Examiner will set eight questions fairly distributed & covering the whole syllabus. Students will be required to attempt any five questions in the duration of 03 hours.

### ECL-725 (iii) MEMS and IC Integration

Overview of CMOS process in IC fabrication, MEMS system-level design methodology, Equivalent Circuit representation of MEMS, signal-conditioning circuits, and sensor noise calculation.

Pressure sensors with embedded electronics(Analog/Mixed signal): Accelerometer with transducer, Gyroscope, RF MEMS switch with electronics, Bolo meter design.

RF MEMS, and Optical MEMS

Text/References:


Note: Examiner will set eight questions fairly distributed & covering the whole syllabus. Students will be required to attempt any five questions in the duration of 03 hours.
### ECP-726 | Adaptive Signal Processing Lab

List of Experiments:
1. Write matlab statement for algebraic equations.
2. Designing Filters from Windowing techniques.
3. Write matlab programme to find the Power spectral Density.
5. Filter design with the help of matlab filter design tool.
7. Matlab programme for cross correlation and auto correlation.
8. Working with DSP Processor & Hardware.

### ECP-727 | Advanced Communication Lab

Experiments related to theory of subjects related to communication engineering.
THIRD SEMESTER

ELECTIVE-II

The student can opt any one elective from the following list.

<table>
<thead>
<tr>
<th>ECL-731 (i)</th>
<th>Mixed-Signal Design</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.</td>
<td>Analog Filters (Continuous-Time and Switched-Capacitor); Digital Filters.</td>
</tr>
<tr>
<td>5.</td>
<td>Sigma-Delta Converters.</td>
</tr>
</tbody>
</table>

TEXT BOOK:


REFERENCE BOOKS:


Note: Examiner will set eight questions fairly distributed & covering the whole syllabus. Students will be required to attempt any five questions in the duration of 03 hours.


**Introduction to RF and Wireless Technology:** Complexity, design and applications. Choice of Technology.

**Basic concepts in RF Design:** Nonlinearly and Time Variance, intersymbol Interference, random processes and Noise. Definitions of sensitivity and dynamic range, conversion Gains and Distortion.


**Basic blocks in RF systems and their VLSI implementation:** Low Noise Amplifiers design in various technologies, Design of Mixers at GHz frequency range. Various Mixers, their working and implementations, Oscillators: Basic topologies VCO and definition of phase noise. Noise-Power trade-off. Resonatorless VCO design. Quadrature and single-sideband generators.

**Radio Frequency Synthesizes:** PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifiers design. Linearisation techniques, Design issues in integrated RF filters. Some discussion on available CAD tools for RF VLSI designs.

**Texts/References:**


**Note:** Examiner will set eight questions fairly distributed & covering the whole syllabus. Students will be required to attempt any five questions in the duration of 03 hours.
ECL-731 (iii)  |  VLSI Testing & Testability

The need for testing, the problems of digital and analog testing, Design for test, Software testing

Faults in Digital circuits: General introduction, Controllability and Observability.. Fault models - Stuck-at faults, Bridging faults, intermittent faults

Digital test pattern generation: Test pattern generation for combinational logic circuits, Manual test pattern generation, Automatic test pattern generation - Roth's D-algorithm, Developments following Roth's D-algorithm, Pseudorandom test pattern generation, Test pattern generation for sequential circuits, Exhaustive, non-exhaustive and pseudorandom 70 test pattern Generation, Delay fault testing

Signatures and self test: Input compression Output compression Arithmetic, Reed-Muller and spectral coefficients, Arithmetic and Reed-Muller coefficients, Spectral coefficients, Coefficient test signatures, Signature analysis and Online self test

Testability Techniques: Partitioning and ad hoc methods and Scan-path testing, Boundary scan and IEEE standard 1149.1, Offline built in Self Test (BIST), Hardware description languages and test

Testing of Analog and Digital circuits: Testing techniques for Filters, A/D Converters, RAM, Programmable logic devices and DSP

Text:

1. VLSI Testing: digital and mixed analogue digital techniques Stanley L. Hurst
Pub:Inspec/IEE, 1999

Note: Examiner will set eight questions fairly distributed & covering the whole syllabus. Students will be required to attempt any five questions in the duration of 03 hours.

Note: Examiner will set eight questions fairly distributed & covering the whole syllabus. Students will be required to attempt any five questions in the duration of 03 hours.
Need for low power VLSI chips. Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices.

**Device & Technology Impact on Low Power**
Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

**Power estimation**
Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems. Monte Carlo simulation. Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

**Low Power Design**
Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic
Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.
Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network

**Text:**

**References:**

**Note:** Examiner will set eight questions fairly distributed & covering the whole syllabus. Students will be required to attempt any five questions in the duration of 03 hours.
Introduction to wireless technologies: WAP services, Serial and Parallel Communication, Asynchronous and synchronous Communication, FDM, TDM, TFM, Spread spectrum technology

Introduction to Bluetooth: Specification, Core protocols, Cable replacement protocol

Bluetooth Radio: Type of Antenna, Antenna Parameters, Frequency hoping

Bluetooth Networking: Wireless networking, wireless network types, devices roles and states, adhoc network, scatternet

Connection establishment procedure, notable aspects of connection establishment, Mode of connection, Bluetooth security, Security architecture, Security level of services, Profile and usage model: Generic access profile (GAP), SDA, Serial port profile, Secondary bluetooth profile


Programming with Java: Java Programming, J2ME architecture, Javax.bluetooth package Interface, classes, exceptions, Javax.obex Package: interfaces, classes

Bluetooth services registration and search application, bluetooth client and server application. Overview of IrDA, HomeRF, Wireless LANs, JINI

Text:

1. Bluetooth Technology by C.S.R. Prabhu and A.P. Reddi; PHI

Note: Examiner will set eight questions fairly distributed & covering the whole syllabus. Students will be required to attempt any five questions in the duration of 03 hours.
ECL-731 (vii)  Hardware & Software Co-Design

Introduction: Motivation hardware & software co-design, system design consideration, research scope & overviews Hardware Software background: Embedded systems, models of design representation, the virtual machine hierarchy, the performance modeling, Hardware Software development,

Hardware Software co-design research: An informal view of co-design, Hardware Software tradeoffs, crosses fertilization, typical co-design process, co-design environments, limitation of existing approaches, ADEPT modeling environment.


Methodology for co-design: Amount of unification, general consideration & basic philosophies, a framework for co-design.

Unified representation for Hardware & Software: Benefits of unified representation, modeling concepts

An abstract Hardware & Software model: Requirement & applications of the models, models of Hardware Software system, an abstract Hardware Software models, generality of the model

Performance evaluation: Application of the abstract Hardware & Software model, examples of performance evaluation

Object oriented techniques in hardware design: Motivation for object oriented technique, data types, modeling hardware components as classes, designing specialized components, data decomposition, Processor example.

Text


References


Note: Examiner will set eight questions fairly distributed & covering the whole syllabus. Students will be required to attempt any five questions in the duration of 03 hours.
Introduction: Elements of Digital Communication system, Bandpass and Lowpass signal representation, Comparison between analog & Digital Communication, Performance parameters of Digital Communication, Concept of Constellation, BER, etc.

Digital Modulation Techniques: Mathematical expressions, transmitter & receiver structure of ASK, FSK, BPSK, QPSK, M-ary PSK, MSK, QAM.


Information Theory & Coding: Measures of information, Entropy, Information rate, Channel Capacity, Source Coding (Huffman, Shannon-Fano, Lempel-Ziv), Channel coding (Block codes, Convolution codes, Turbo codes).

Books:
4. Digital Communications: Fundamentals and applications- Bernard Sklar, PHI

Note: Examiner will set eight questions fairly distributed & covering the whole syllabus. Students will be required to attempt any five questions in the duration of 03 hours.
1. Orbital Parameters:
Orbital parameters, Orbital perturbations, Geo stationary orbits, Low Earth and Medium orbits. Frequency selection, Frequency co-ordination and regulatory services, Sun transit outages, Limits of visibility, Attitude and orientation control, Spin stabilization techniques, Gimbal platform

2. Link Calculations:
Space craft configuration, Payload and supporting subsystems, Satellite uplink -down link power budget, C/No, G/T, Noise temperature, System noise, Propagation factors, Rain and ice effects, Polarization calculations

3. Access Techniques:
Modulation and Multiplexing: Voice, Data, Video, Analog and Digital transmission systems, multiple access techniques: FDMA, TDMA, T1-T2 carrier systems, SPADE, SS-TDMA, CDMA, Assignment Methods, Spread spectrum communication, Compression-Encryption and Decryption techniques

4. Earth Station Parameters:
Earth station location, propagation effects of ground, High power transmitters-Klystron Crossed field devices, Cassegrania feeds, Measurements on G/T and Eb/No

5. Satellite Applications:
INTELSAT Series, INSAT, VSAT, Remote sensing, Mobile satellite service: GSM, GPS, INMARSAT, Satellite Navigation System, Direct to Home service (DTH), Special services, E-mail, Video conferencing and Internet connectivity

Books:
5. K.Feher, Digital communication satellite / Earth Station Engineering, prentice Hall Inc, New Jersey, 1983

Note: Examiner will set eight questions fairly distributed & covering the whole syllabus. Students will be required to attempt any five questions in the duration of 03 hours.
Advance VLSI Design Lab
ECP-732

List of Experiments

1. To study the characteristics of Common gate configuration in mentor graphic Design architecture.
2. To study the characteristics of Common source configuration in mentor graphic Design architecture.
3. To study the characteristics of Common drain configuration in mentor graphic Design architecture.
4. To study the characteristics of switched capacitor integrator amplifier in mentor graphic Design architecture.
5. To study the characteristics of two stage MOS OpAmp configuration in mentor graphic Design architecture.
6. To study the characteristics of MOS Cascode configuration in mentor graphic Design architecture.
7. To study the characteristics of MOS Folded-cascode operational amplifiers configuration in mentor graphic Design architecture.
8. To study the characteristics of Source Follower configuration in mentor graphic Design architecture.
9. To study the characteristics of OTA Amplifiers configuration in mentor graphic Design architecture.
10. To study the characteristics of Voltage controlled oscillator and Comparators, configuration in mentor graphic Design architecture.
11. Design of VCO, DCOs and PLL circuits.
12. Layout design of circuits and verification of designs through simulation.

Communication System Design Lab
ECP 733

Experiments related to communication system designs using OPTSIM/MATLAB software.

ECD-730 | Thesis – Part I

The Thesis work should be of Research nature only and it should be started during the third semester and the candidate must do the following:

1. Literature Survey
2. Problem Formulation

Around 40% of the Thesis work should be completed in this semester. The remaining 60% work will be carried out in the fourth semester. Each student is required to submit a detailed report about the work done on topic of Thesis as per the guidelines decided by the department. The Thesis work is to be evaluated through Presentations and Viva-Voce
during the semester and at the end of semester as per the guidelines decided by the department from time to time.

**FOURTH SEMESTER**

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<th>ECD-740</th>
<th>Thesis – Part II</th>
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<td>Around 40% of the Thesis work should be completed in third semester. The remaining 60% work will be carried out in this semester. Each student is required to submit a detailed Thesis report about the work done (III Sem + IV Sem) on topic of Thesis as per the guidelines decided by the department. The Thesis work is to be evaluated through Presentations and Viva-Voce during the semester and Final evaluation will be done at the end of semester as per the guidelines decided by the department from time to time.</td>
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The candidate has to present/publish one paper in national/international conference/seminar/journal of repute is must before submission. Research work should be carried out at GJUS & T, Hisar. However candidate may visit research labs/institutions with the due permission of chairperson on recommendation of supervisor concerned.